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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,929	06/26/2003	Dong Hoon Lee	8734.208.00 US	3404

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EXAMINER	
NGUYEN, THANH T	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 04/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/603,929	LEE ET AL.	
	Examiner	Art Unit	
	Thanh T. Nguyen	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *1-8* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 9-22 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 9, 10-13, 18, 19, 21-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Ueda et al. (U.S. Patent No. 6,714,266).

Referring to figures 2a-3d, Ueda et al. teaches a method of fabricating a contact line structure for a liquid crystal display device, comprising:

forming a metal line (17, Aluminum or tungsten) on an array substrate (1);

forming a silicide layer (18, see figure 3c) on the metal line direct contact (see col. 7, lines 1-20) with at least a first surface portion of the metal line and the silicide layer is formed in a different layer from the metal line (see figure 3c);

forming an insulating layer (9, see figure 3d) having a contact hole exposing a first portion of the silicide layer, and

forming a transparent conducting terminal (19, ITO, see figure 3D) in and on the contact hole,

wherein the insulating layer (9) is adjacent to the contact hole (see figure 3d).

Regarding to claim 10, wherein the steps of forming the metal line and the silicide layer include: depositing a metal material (17, see figure 3c, col. 7, lines 1-20) on the array substrate;

forming the silicide layer (18, see figure 3c) on the metal material; and

forming the metal line (17, see figure 3c) by etching the silicide layer and the metal material.

Regarding to claim 11, wherein the steps of forming the metal line and the silicide layer include: depositing a metal material (17) on the array substrate;

forming the metal line (17, patterning) by etching the metal material; and

forming the silicide layer (18, see figure 3c) to cover the first portion of the metal line.

Regarding to claim 12, wherein the step of forming the silicide layer (18) is performed before the step of forming an insulating layer (19, see figure 3c-3d).

Regarding to claim 13, wherein the metal line includes one of chrome Cr, molybdenum Mo, tungsten W, titanium Ti, tantalum Ta, and a conductive metal alloy (see col. 7, lines 3-20).

Regarding to claim 14, the step of forming a silicide layer includes a plasma process using island group gas containing silicon ()

Regarding to claim 18, wherein the transparent conducting terminal includes a transparent conducting oxide (18, ITO, see figure 3d).

Regarding to claim 19, wherein the step of forming a metal line includes simultaneous steps of forming a gate line (GL) arranged along a first direction on the array substrate, forming a gate electrode (7) protruding from the gate line, and forming a storage lower electrode in a storage capacitor region (2/3/5a, see figure 2b) of an adjacent gate line (see figures 2b).

Regarding to claims 21-22, transparent conducting terminal is a gate pad terminal that simultaneously formed a data pad terminal and a pixel electrode (19, see figure 3d).

Claims 9, 11, 14, 18, 21-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Sung (U.S. Patent No. 5,978,058).

Referring to figures 1, Sung teaches a method of fabricating a contact line structure for a liquid crystal display device, comprising:

forming a metal line (11) on an array substrate;

forming a silicide layer (13, see figure 1) on the metal line direct contact (see col. 5, lines 1-10) with at least a first surface portion of the metal line and the silicide layer is formed in a different layer from the metal line (see figure 1);

forming an insulating layer (7, see figure 1) having a contact hole exposing a first portion of the silicide layer, and

forming a transparent conducting terminal (14, ITO, see figure 1) in and on the contact hole,

wherein the insulating layer (7) is adjacent to the contact hole (see figure 1).

Regarding to claim 10, wherein the steps of forming the metal line and the silicide layer include: depositing a metal material (11, see figure 1) on the array substrate;

forming the silicide layer (13, see figure 1) on the metal material; and

forming the metal line (11, see figure 1) by etching the siliçide layer and the metal material.

Regarding to claim 11, wherein the steps of forming the metal line and the silicide layer include: depositing a metal material (11) on the array substrate;

forming the metal line (11, patterning) by etching the metal material; and

forming the silicide layer (13, see figure 1) to cover the first portion of the metal line.

Regarding to claim 12, wherein the step of forming the silicide layer (13) is performed before the step of forming an insulating layer (7, see figure 1).

Regarding to claim 14, the step of forming a silicide layer includes a plasma process using island group gas containing silicon (see col. 5, lines 55-67).

Regarding to claim 18, wherein the transparent conducting terminal includes a transparent conducting oxide (14, ITO, see figure 1).

Regarding to claims 21-22, transparent conducting terminal is a gate pad terminal that simultaneously formed a data pad terminal and a pixel electrode (10/14, see figure 1).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 14-17, 20 are stand rejected under 35 U.S.C. 103(a) as being unpatentable over Ueda et al. (U.S. Patent No. 6,714,266) as applied to claims 9-13, 18, 19, 21-22 above or Sung (U.S. Patent No. 5,978,058) as applied to claims 9, 11, 14, 18, 21-22 above in view of Admitted Prior Art of the Present Invention (pages 2-7) and Chowdhury (U.S. patent No. 6,268,289).

Ueda et al., or Sung teaches all of the limitations as described in the claimed invention above. However, the reference does not teach forming the metal line and the silicide layer by forming the metal line by etching the silicide layer and the metal material, forming a silicide layer includes a plasma process using a silane group gas containing silicon, the plasma process is performed at a power of about 100Watt or less, a pressure of about 110Pa, a temperature of about 250^0C to about 500^0C, and a gas flow of about 100SCCM or less, the silane group gas is one of SiH_4, Si_2H_6, and Si_3H_8, the insulating layer includes one of an organic insulating material group containing Benzocyclobutene (BCB) or a photoacrylic resin, forming a gate insulating layer on the gate electrode, forming an active layer on the gate insulating layer above the gate electrode, forming a data line perpendicular to the gate line to define a pixel region, simultaneously forming a data pad at one end of the data line, and forming a source electrode above the gate electrode to overlap with a first side of the active layer when forming the data

line; and simultaneously forming a drain electrode to overlap a second side of the active layer at a fixed interval apart from the source electrode, and forming the storage upper electrode in the storage capacitor region of the adjacent gate line when forming the data line.

The Admitted Prior Art of the Present Invention (pages 2-7) teaches the insulating layer includes one of an organic insulating material group containing Benzocyclobutene (BCB) or a photoacrylic resin (see paragraph#8). The Admitted Prior Art of the Present Invention (pages 2-7) also teaches forming a gate insulating layer (see para# 6) on the gate electrode (11b); forming an active layer (13) on the gate insulating layer above the gate electrode; forming a data line (14) perpendicular to the gate line to define a pixel region (see para# 7); simultaneously forming a data pad (17a/17b, para# 8) at one end of the data line, and forming a source electrode (14b, para# 7) above the gate electrode to overlap with a first side of the active layer when forming the data line; and simultaneously forming a drain electrode (14c, para# 7) to overlap a second side of the active layer at a fixed interval apart from the source electrode, and forming the storage upper electrode in the storage capacitor region of the adjacent gate line when forming the data line.

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would forming the insulating layer by using organic material group containing Benzocyclobutene (BCB) or a photoacrylic resin, and the pixel array regions of an array substrate in process of Ueda et al., or Sung as taught by the admitted prior art because the process is known in the art to form a display device to improve image quality, such as fineness, brightness, and large-size.

Chowdhury et al. teaches forming a silicide layer includes a plasma process using a silane group gas containing silicon , wherein the silane group gas is one of SiH_4, Si_2H_6, and Si_3H_8 (see col. 6, lines 5-16).

Therefore, it would have been obvious to one of ordinary skill in the requisite art at the time of the invention was made would forming a silicide layer by using plasma silane (SiH4) in process of Ueda et al., or Sung as taught by Chowdhury et al. because the process would forming a silicide layer only on selective region of the semiconductor device.

The power range, pressure, the temperature range, the flowrate range are considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As noted in In re Aller, the selection of reaction parameters such as temperature and concentration would have been obvious:

> Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art...such ranges are termed Acritical ranges and the applicant has the burden of proving such criticality.... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.
> *In re Aller 105 USPQ233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).*

Therefore, one of ordinary skill in the requisite art at the time the invention was made would have used any power range, pressure, the temperature range, the flowrate range suitable to the method in process of Ueda et al., or Sung in order to optimize the process.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached on (571) 272-1702. The fax phone number for this Group is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956 (**See MPEP 203.08**).

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pairdirect.uspto.gov. Should you have questions on access to thy Private PAIR system, contact the Electronic Business center (EBC) at 866-217-9197 (toll-free).

Thanh Nguyen
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Patent Examining Group 2800

TTN